POLITECNICO DI MILANO

PhD in INGEGNERIA DELL'INFORMAZIONE / INFORMATION TECHNOLOGY - 41st cycle

Research Area n. 1 - Computer Science and Engineering

BORSE TEF Research Field: RECONFIGURABLE HARDWARE ACCELERATORS FOR ARTIFICIAL INTELLIGENCE ON FPGAS

Monthly net income of PhDscholarship (max 36 months)
1800.0 In case of a change of the welfare rates during the three-year period, the amount could be modified.

Context of the research activity	
Motivation and objectives of the research in this field	The growth of artificial intelligence (AI) in recent years has fueled a surge in demand for specialized hardware accelerators. Companies like NVIDIA have become central players in this landscape, with GPUs powering much of today’s large-scale AI training and inference. This momentum has spurred a broader industry-wide shift toward dedicated AI acceleration solutions, including emerging custom chips and application-specific architectures, to meet the increasing need for performance, scalability, and efficiency. However, traditional architectures—such as CPUs and GPUs—often fall short in meeting modern AI requirements, particularly in terms of energy efficiency and adaptability. Field-Programmable Gate Arrays (FPGAs) offer a flexible and energy-conscious alternative. Their reconfigurable nature allows the creation of custom hardware architectures tailored to specific AI workloads, delivering high performance with significantly lower power consumption across the entire computing spectrum—from datacenters to the edge.Unlike fixed-function ASICs or power-intensive GPUs, FPGAs can be reprogrammed to support evolving AI models, making them ideal for datacenter environments where agility, sustainability, and long-term efficiency are crucial. Improving energy efficiency at this scale is not only economically advantageous—it is vital to

	reduce the environmental footprint of digital infrastructure and to meet global climate targets. Major cloud providers such as Microsoft Azure and AWS have already invested in FPGA-based infrastructure, allocating significant resources to develop and deploy these solutions at scale. This demonstrates not only a belief in the potential of FPGAs for AI, but also a market signal that this direction is gaining momentum and industry-wide relevance. At the edge, where devices such as drones, sensors, and mobile systems operate under tight resource constraints, FPGAs enable real-time, low-power AI processing tailored to each application's needs. Companies like AMD and Intel provide FPGA platforms explicitly targeting edge AI. Industrial players such as Siemens and Bosch leverage FPGAs for smart sensors and real-time control systems, while DJI and defense contractors utilize them in autonomous drones for onboard inference and navigation. In these contexts, FPGAs provide a unique blend of adaptability, low latency, and efficient resource utilization that traditional processors and even GPUs struggle to match. This research aligns with national strategic goals as the PNRR, which prioritizes digital innovation, technological sovereignty, and sustainability. It also fits within broader EU initiatives as the European Green Deal and the Innovation Fund to support low-carbon technologies and energy-efficient digital solutions, with the objective of net zero emissions of greenhouse gases by 2050. FPGA-based AI accelerators contribute to these objectives by enabling secure, efficient, and future-proof computing solutions across sectors.
Methods and techniques that will be developed and used to carry out the research	The work will focus on creating novel design methodologies and architectural solutions that exploit the flexibility of reconfigurable hardware to meet the growing computational demands of artificial intelligence—while minimizing energy consumption. The candidate will investigate a combination of hardware and software co-design techniques to optimize power efficiency, performance, and adaptability, targeting both edge and datacenter use cases where resource constraints and sustainability are critical. A key focus will be on the development of accelerators that leverage the inherent

	flexibility of FPGAs to tailor computational pipelines for specific AI workloads. This will include the exploration of innovative design paradigms, such as custom dataflow architectures and hardware/software co-design strategies, to push the boundaries of accelerator performance while maintaining efficiency. Prototyping and iterative refinement will be central to the approach, ensuring that proposed accelerator designs are rigorously validated against practical performance and energy benchmarks. The methodology will evolve in response to rapid developments in AI models, frameworks, and deployment scenarios. Particular attention will be given to ensuring that the proposed accelerator designs remain compatible with real-world requirements, including scalability, interoperability with industry-standard toolchains, and ease of integration into existing systems. By aligning with current and emerging trends in AI hardware and software, the research will contribute solutions that are both forward-looking and practically applicable in industrial contexts.
Educational objectives	The PhD program is designed to equip the candidate with a comprehensive and interdisciplinary skill set over hardware design, artificial intelligence, and system-level optimization. The primary educational objective is to develop advanced expertise in the design, implementation, and evaluation of low-power, high-performance hardware accelerators using reconfigurable computing platforms such as FPGAs. In parallel, the candidate will be trained to critically analyze the evolving landscape of AI hardware, understand emerging application requirements, and evaluate trade-offs between performance, power consumption, scalability, and flexibility. Through exposure to both academic research and industrial practice, including a hands-on internship and international collaboration, the candidate will build the capacity to independently conduct high-impact research and contribute to innovation in real-world contexts.The program also aims to develop soft skills essential for future careers in academia, industry, or entrepreneurship, including scientific communication, project management, collaboration, and intellectual property strategy.

Job opportunities	The PhD candidate will develop deep technical expertise in designing high-performance, energy-efficient AI accelerators, along with a strong understanding of market trends and application needs, equipping them to deliver innovative and impactful solutions.Upon completing the PhD, the candidate will be well positioned to pursue a range of career paths. These include joining leading tech companies or semiconductor firms working on next-generation AI hardware, continuing in academic or industrial research with a focus on energy-efficient computing, or contributing to innovation through technology transfer and IP licensing. If the developed solutions demonstrate clear market potential, founding a startup will also be a viable and supported option, particularly given the current investment momentum and strategic interest in AI hardware across Europe and globally.
Composition of the research group	1 Full Professors 0 Associated Professors 1 Assistant Professors 3 PhD Students
Name of the research directors	Prof. Marco Domenico Santambrogio

Contacts
marco.santambrogio@polimi.it

Additional support - Financial aid per PhD student per year (gross amount)	
Housing - Foreign Students	--
Housing - Out-of-town residents	--

Scholarship Increase for a period abroad	
Amount monthly	900.0 €
By number of months	6

Additional information: educational activity, teaching assistantship, computer availability, desk availability, any other information
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EDUCATIONAL ACTIVITIES (purchase of study books and material, including computers,funding for participation in courses, summer schools, workshops and conferences): financial aid per PhD student.

TEACHING ASSISTANTSHIP: availability of funding in recognition of supporting teaching activities by the PhD student.
There are various forms of financial aid for activities of support to the teaching practice. The PhD student is encouraged to take part in these activities, within the limits allowed by the regulations.

COMPUTER AVAILABILITY:
1st year: Yes
2nd year: Yes
3rd year: Yes