POLITECNICO DI MILANO

PhD in INGEGNERIA DELL'INFORMAZIONE / INFORMATION TECHNOLOGY - 40th cycle

Research Area n. 1 - Computer Science and Engineering

PNRR 630 Research Field: DESIGN METHODOLOGIES FOR DIGITAL IN-MEMORY COMPUTING IN MICROPROCESSOR ARCHITECTURES TO ACCELERATE DEEP LEARNING

Monthly net income of PhDscholarship (max 36 months)
€ 1500.0 In case of a change of the welfare rates during the three-year period, the amount could be modified.

Context of the research activity	
Motivation and objectives of the research in this field	Digital In-Memory Computing (D-IMC) is an innovative paradigm to accelerate Deep Learning applications on edge devices. This has the benefit of reducing the data traffic and improve the energy efficiency beyond the limits of traditional digital designs. D-IMC can perform digital calculation directly in SRAM based memory macros or even in different emerging memories technologies, such as different kinds of resistive memories. SRAM based digital IMC architectures, however, have the advantage versus NVM-based memories that neural network's weights data can be quickly loaded and replaced (if required) and most of these structures can also be repurposed as conventional memory system when this functionality is not in use. It is also crucial to define and optimize the System-on-Chip architecture by assessing the tradeoffs between performance, area, and power consumption while considering constraints unique to the Deep Learning domain because of its significant market volumes and complexity. Main objective of this PhD research is to devise an innovative design methodology for system-level modeling and design space exploration (DSE) that can achieve these tradeoffs. There are some exploration options on how D-IMC tiles can be integrated into a System-on-Chip foredge devices: approaches that couple such D-IMC tiles either loosely- or tightly-coupled

	to the Central Processing Unit. Another step further in the PhD program is the integration into a microprocessor data-path which could use the functionality provided by the D-IMC tiles similarly to the functional units used for arithmetic operations such as a Multiply-Accumulator (MAC) unit. In this context, the PhD thesis will investigate design space exploration of various coupling and integration approaches together with an in-deep study of the implications on the required instruction set extensions, programming tool support, achievable performance, and power efficiency. During the PhD program, all these topics will be further investigated, and an integration of D-IMC tiles in existing microprocessors (like the open-hardware RISC-V architecture) could be specified at the instruction set level and integrated in the processor pipeline (such as tightly-coupled memories replacement or additional data-path) to validate what processing performance and power efficiency level could be achieved that outperform the current state-of-the-art, while preserving system cost within the budget required for TinyML edge devices.
Methods and techniques that will be developed and used to carry out the research	- Develop design techniques to combine DIMC tiles either loosely- or tightly-coupled to the central processing unit. - Develop design techniques of a RISC-V based data-path and their function units to directly exploit the functionality provided by DIMC tiles. - System-level modeling and exploration techniques to evaluate design tradeoffs and tune System-on-Chip platforms with respect to various metrics associated with a system configuration such as performance, area and power consumption.
Educational objectives	Acquire and/or consolidate knowledge and/or practical skills around: ¿ Modeling and simulation at the system-on-chip level ¿ Hardware architectural definition and exploration ¿ Design of experiments and Machine-Learning models ¿ Analysis and design for power/performance tradeoffs.
Job opportunities	The research proposal addresses an output profile that responds to the needs of the edge-computing industry fortechnical experts in the design and the development of

	next generation digital systems to accelerate Deep Learninga pplications.
Composition of the research group	2 Full Professors 2 Associated Professors 0 Assistant Professors 3 PhD Students
Name of the research directors	Prof.ssa Cristina Silvano

Contacts
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Additional support - Financial aid per PhD student per year (gross amount)	
Housing - Foreign Students	--
Housing - Out-of-town residents (more than 80Km out of Milano)	--

Scholarship Increase for a period abroad	
Amount monthly	750.0 €
By number of months	6

National Operational Program for Research and Innovation	
Company where the candidate will attend the stage (name and brief description)	STMICROELECTRONICS S.R.L.
By number of months at the company	6
Institution or company where the candidate will spend the period abroad (name and brief description)	ETH Zurich, Research group of prof. Luca Benini - Zurich, Switzerland
By number of months abroad	6

Additional information: educational activity, teaching assistantship, computer availability, desk availability, any other information

EDUCATIONAL ACTIVITIES (purchase of study books and material, including computers, funding for participation in courses, summer schools, workshops and conferences): financial aid per PhD student.

TEACHING ASSISTANTSHIP: availability of funding in recognition of supporting teaching activities by the PhD student. There are various forms of financial aid for activities of support to the teaching practice.
The PhD student is encouraged to take part in these activities, within the limits allowed by the regulations.

COMPUTER AVAILABILITY:
1st year: Yes

2nd year: Yes
3rd year: Yes