



# PhD in INGEGNERIA DELL'INFORMAZIONE / INFORMATION TECHNOLOGY - 38th cycle

Research Area n. 2 - Electronics

PNRR\_352 Research Field: **ADVANCED CODING FOR DIFFERENTIAL PCM MEMORIES**

**Monthly net income of PhDscholarship (max 36 months)**

**€ 1400.0**

In case of a change of the welfare rates during the three-year period, the amount could be modified.

## Context of the research activity

**Motivation and objectives of the research in this field**

The automotive industry is undergoing a deep transformation, driven by disruptive technological innovation in the fields of Electrification. Despite the diverse areas of innovation, they rely on Microcontrollers to perform safe computation and secure data transmission. As the applications evolve, the demand on high computation, lower power consumption and larger memory footprint is driving the automotive MCU technology development. Embedded Non Volatile Memory (e\_NVM) is one of the most challenging topics: MCUs are requested to store more data to host more complex firmware. Real time requires fast access to code memory and more complex security software requires peculiar NVM array partitioning. In case of advanced CMOS platform, facing huge process complexity growth while shrinking, among all the resistive memories proposed nowadays as innovative solutions able to replace Floating Gate cells, PCM is the only one demonstrated to be compliant simultaneously with automotive requirements. In NVM area density is a key enabler. In PCM memory the bit is differential so 2 cells are needed for a single bit (to sustain the physical intrinsic drift of the I-V characteristic). An adequate error correcting code (ECC) is also need to get a proper BER. In this scenario, the main goal of the PhD research is to elaborate an innovative coding for differential memory,



	preserving the intrinsic robustness (in term of reliability) of the symbols. This encompass NVM state definition, sense amplifiers for reading the cells and finally ECC detection and correction. Ultimate aim is to save a relevant fraction of the physical memory array ( > 25%) while preserving the same information content of a pure differential memory approach (2 cells - 1 bit).
<b>Methods and techniques that will be developed and used to carry out the research</b>	NVM cell reading for fast access time Cells current processing for multi (>3) cells simultaneous reading ECC coding develop for multi bit (>1b) symbols ECC implementation for fast combinatorial decoding access
<b>Educational objectives</b>	To acquire and/or consolidate knowledge and/or practical skills around: Design and verification (analog & digital) ECC coding (matlab & Verilog) Modeling and simulation at the system-on-chip level
<b>Job opportunities</b>	The research proposal addresses an output profile that responds to the needs of the automotive industry for technical experts in the design and the development of next generation of automotive NVM solutions.
<b>Composition of the research group</b>	1 Full Professors 0 Associated Professors 0 Assistant Professors 10 PhD Students
<b>Name of the research directors</b>	Prof. Daniele Ielmini

<b>Contacts</b>	
daniele.ielmini@polimi.it, 02 2399 6120, <a href="https://ielmini.faculty.polimi.it/">https://ielmini.faculty.polimi.it/</a>	

<b>Additional support - Financial aid per PhD student per year (gross amount)</b>	
<b>Housing - Foreign Students</b>	--
<b>Housing - Out-of-town residents (more than 80Km out of Milano)</b>	--



Scholarship Increase for a period abroad	
Amount monthly	700.0 €
By number of months	6

National Operational Program for Research and Innovation	
Company where the candidate will attend the stage (name and brief description)	STMicroelectronics Italia
By number of months at the company	6
Institution or company where the candidate will spend the period abroad (name and brief description)	STMicroelectronics, France
By number of months abroad	6

**Additional information: educational activity, teaching assistantship, computer availability, desk availability, any other information**

**Attinenza alla tematiche, alle missioni/componenti prescelte del bando PNRR v. D.M. 352, art.6**

Le memorie a cambiamento di fase (phase change memory, PCM) sono una tecnologia di memoria embedded in grado di raggiungere alte densità di integrazione di memoria e di ridurre drasticamente i consumi energetici per il calcolo e l'immagazzinamento di dati. Pertanto, esse rappresentano una tecnologia abilitante per tutti i sistemi microelettronici, quali i microcontrollori, i microsensori ed i componenti di potenza, che trovano svariate applicazioni nel settore manifatturiero, nell'automotive e nella domotica. Pertanto, questo progetto di dottorato risponde pienamente alla missione M1 "Digitalizzazione, innovazione, competitività, cultura e turismo", ed in particolare alla componente M1C2 "Digitalizzazione, innovazione e competitività nel sistema produttivo". Nell'ambito di questa componente, la codifica avanzata della PCM oggetto di questo dottorato permetterà di sviluppare nuovi microcontrollori a più alta capacità di memoria, a minore consumo energetico e a minore costo, che abiliteranno una più massiccia digitalizzazione dei processi produttivi, in termini di intelligenza artificiale inserita nell'automazione industriale, come la manutenzione preventiva di macchinari e la pianificazione logistica dei flussi produttivi, in modo da rendere più efficiente, più veloce, più economico e quindi più competitivo il sistema produttivo.

**Impresa, presso cui si svolgerà l'attività esterna**

STMicroelectronics Italia

**Ente, università, azienda, centro di ricerca presso cui si svolgerà il periodo di studio e ricerca all'estero.**

STMicroelectronics, France

**All information regarding educational activities, personal funding, regulations and obligations of Ph.D. candidates are available on the web**



site <https://dottoratoit.deib.polimi.it/>