



# PhD in INGEGNERIA DELL'INFORMAZIONE / INFORMATION TECHNOLOGY - 39th cycle

Research Area n. 1 - Computer Science and Engineering

**THEMATIC Research Field: DESIGN METHODOLOGIES USING AI FOR DIGITAL AND MIXED-SIGNAL CIRCUITS**

**Monthly net income of PhDscholarship (max 36 months)**

**€ 1400.0**

In case of a change of the welfare rates during the three-year period, the amount could be modified.

**Context of the research activity**

**Motivation and objectives of the research in this field**

To optimize their spending and meet the time-to-market, chip designers started looking at the artificial intelligence (AI) as the viable solution to effectively make automatic and smart many of the tasks in the hardware design flow, e.g., place-and-route, chip verification tasks, and design space exploration [1,2].

However, the use of machine learning techniques to optimize the production costs as well as the power, performance, and area metrics in the hardware design flow represents a complex and highly multi-disciplinary research topic that requires skills in (1) the design of software architecture to automate parts of the hardware design flow, (2) the design of machine learning algorithms targeting specific tasks in the hardware design flow, and (3) the use of proper hardware design and verification methodologies.

The research aims to advance the state of the art in the design, verification, and test methodologies for modern digital and mixed-signal circuits using machine learning techniques.

1] [https://www.cadence.com/en\\_US/home/tools/digital-design-and-signoff/soc-implementation-and-floorplanning/cerebrus-intelligent-chip-explorer.html](https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/soc-implementation-and-floorplanning/cerebrus-intelligent-chip-explorer.html)

[2] <https://www.synopsys.com/ai/chip-design.html#dso>



<b>Methods and techniques that will be developed and used to carry out the research</b>	Design methodologies using machine learning to optimize the design, verification, and test of complex digital and mixed-signal circuits.
<b>Educational objectives</b>	The student will acquire strong skills in hardware design (Verilog/Systemverilog), the design and implementation of software architectures to create complex simulation, verification frameworks also integrating with commercial CAD tools, and machine learning solutions targeting the optimization of the hardware design flow.
<b>Job opportunities</b>	Recent graduates in this field have been hired by major semiconductor and technology companies. Post-doc research opportunities are also available. Cooperation with other academic institutions and start-up at PoliMI can open additional job opportunities.
<b>Composition of the research group</b>	0 Full Professors 6 Associated Professors 7 Assistant Professors 6 PhD Students
<b>Name of the research directors</b>	Prof. Davide Zoni

Contacts
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Additional support - Financial aid per PhD student per year (gross amount)	
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<b>Housing - Foreign Students</b>	--
<b>Housing - Out-of-town residents (more than 80Km out of Milano)</b>	--

Scholarship Increase for a period abroad	
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<b>Amount monthly</b>	700.0 €
<b>By number of months</b>	6

Additional information: educational activity, teaching assistantship, computer availability, desk availability, any other information
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EDUCATIONAL ACTIVITIES (purchase of study books and material, including computers, funding for participation in courses, summer schools, workshops and conferences): financial aid per PhD student.
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TEACHING ASSISTANTSHIP: availability of funding in recognition of supporting teaching activities by the PhD student There are various forms of financial aid for activities of support to the teaching practice. The PhD student is encouraged to take part in these activities, within the limits allowed by the regulations.

COMPUTER AVAILABILITY: individual use.

DESK AVAILABILITY: individual use.

List of Universities, Companies, Agencies and/or National or International Institutions that are cooperating in the research:

1. Infineon - IT
2. Infineon - AT
3. E4 - IT
4. CINI HPC-KTT Lab - IT