PhD In
Information Technology

Research Area n. 1 Title: Computer Science and Engineering

Research Field: “Hardware/Software Codesign Methodologies for FPGA-based High Performance Computing Infrastructure”

Scholarships and Financial support	
Monthly net income of PhD scholarship (max 36 months)	€. 1.200 (In case of a change of the welfare rates during the three-year period, the amount could be slightly modified)
Number of scholarships	1
Beginning of PhD	1/5/2017
Deadline for application	13/03/2017
Context of the research activity	
Motivations and objectives of the research in this field	To handle the stringent performance requirements of future exascale High Performance Computing (HPC) applications, HPC systems will need ultra-efficient heterogeneous compute nodes. Some of these nodes will be high performance CPU nodes but other nodes will have to be targeted to specific applications and maximally exploit low-level parallelism. Reconfigurability of these hardware nodes is therefore required and, for applications that significantly change their behaviour during their execution, run-time reconfiguration will be an important asset of such hardware nodes. Within this context, the objectives of this research will be the definition of novel hardware nodes exploiting dynamic reconfiguration and the design of the necessary tools to target these architectures.

Methods and techniques that will be developed and used to carry out the research	The research program aims at creating software/hardware systems that adapts their behaviour basing on the working environment. The systems will be composed of CPUs paired with a hardware accelerator, in particular an FPGA device. FPGAs offers the possibility to be partially or totally configured and reconfigured at runtime. In this way, it is possible to adapt their behaviour basing on inputs of agents that are external to our system (the environment). The program, has as a goal to identify part of the algorithms that would benefit a hardware acceleration on FPGA. Part of the computation, will then be offloaded from the CPU to the FPGA, so that the total execution is more efficient.
Educational objectives	The student will be required to participate in different activities involving research and teaching, managing and mentoring others students for didactical purposes and organise external activities such has the Xilinx PYNQ Hackaton (xph.necst.it)
Job opportunities	Given the renewed interested in FPGA-based systems different job opportunities can be identified. Just to cite few companies with which we are collaborating: Microsoft Research, Xilinx, Maxeler Tech.
Composition of the research group	http://exafpga.necst.it/
Names of the research directors	Marco D. Santambrogio
E-mail address, phone number and web-page	Marco.santambrogio@polimi.it, +393356847022, http://home.deib.polimi.it/santambr/
List of 5 Universities, Companies, Agencies and/or National or International Institutions that are cooperating in the research	1. MIT 2. Berkeley 3. Unicredit 4. Xilinx 5. Maxeler
Additional support	
Educational activities (purchase of study books and material, funding for participation to courses, summer schools, workshops and conferences): financial aid per PhD student per year	2nd year: 1.370 euro per student 3rd year: 1.370 euro per student
Teaching assistantship: availability of funding in recognition of support to teaching activities by the PhD student	There are various forms of financial aid for activities of support to the teaching practice. The PhD student is encouraged to take part in these activities, within the limits allowed by the regulations.
Computer availability:	1st year: *individual use* 2nd year: *individual use* 3rd year: *individual use*

Desk availability:	1st year: *individual use* 2nd year: *individual use* 3rd year: *individual use*